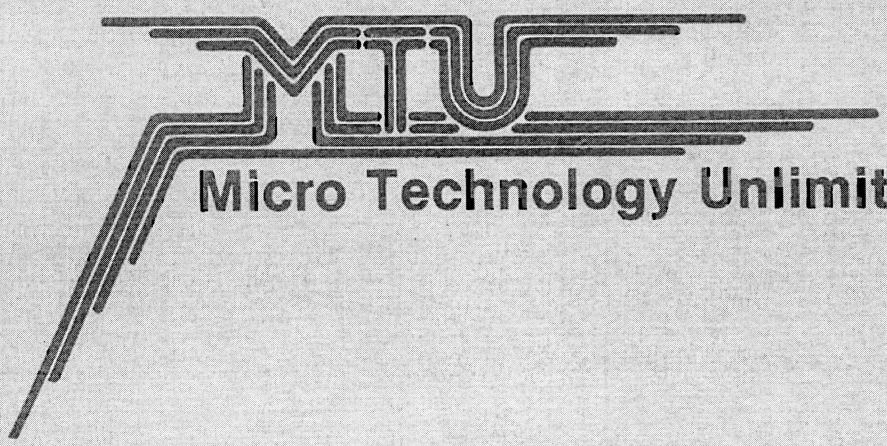


K-1012 PROM/IO BOARD

12K EPROM
4 PARALLEL OUTPUT PORTS WITH 8 CONTROL LINES
SERIAL ASYNCHRONOUS PORT
2708/TMS2716 EPROM PROGRAMMER

FOR 6502 SYSTEMS

MAY, 1979 REVISED JANUARY, 1980

K-1012 UNPACKING AND INSTALLATION

This manual covers the installation and operation of both the K-1012 PROM/IO and K-1012-1 PROM-only board. All comments regarding input/output and PROM programming functions should be ignored if the user has purchased the K-1012-1 board.

The K-1012 PROM/IO is a carefully engineered, manufactured, and tested product that should operate perfectly when handled and installed according to the following instructions. Note that the board is shipped in a black conductive plastic bag. Since MOS integrated circuits are used, damage from static discharge is possible. It is helpful to reduce static by working in an area with concrete floors and a reasonable humidity level. If this is impossible, at least avoid wearing rubber soled shoes and move slowly in the work area. When unpacking or handling the board, touch the screw sticking up in the middle of the heatsink first and release it last. Note that the preceeding comments apply equally to the microcomputer board which of course contains MOS IC's also.

Connection to the microcomputer board should be as indicated in the accompanying chart. The easiest method of connection is with an MTU model K-1005 motherboard/cardfile. Alternatively the user may obtain two 2x22 pin printed circuit board edge connectors (.156" contact spacing) such as the one supplied with the processor and wire them together except for pins 3, 4, 16-20, and X. Wire length should not exceed 4 inches. Plug the processor expansion connector into one of the sockets, make any necessary connections to the application connector, and make any necessary power connections. The K-1012 may then be plugged into the other connector. Note that the K-1012 provides the DECODE ENABLE and VECTOR FETCH signals needed by the KIM-1 for expanded memory. They may be ignored with the SYM and AIM processors.

Note that as shipped the board requires an unregulated voltage between +7 and +12 volts to operate the logic and another unregulated voltage between +14 and +20 volts to operate the memory chips such as provided by the expansion outputs of an MTU K-1000 power supply. The on-board regulators may be bypassed by shorting the two outside pins of each regulator IC together if the user wishes to use a regulated power source. Use of the PROM programmer with a shorted 12 volt regulator is not recommended because the on-board voltage multiplier may not be able to supply the necessary programming power from the lower voltage. The various option jumpers on the board should not be reconfigured until the board is tested. The diagnostic program in the back of this manual assumes the standard jumper configuration which is already installed on assembled boards.

After connecting the processor, the K-1012, and the power supply, the system may be turned on. Pressing RESET on the processor should initiate normal operation. Assuming that one or more PROM's have been installed, look at some PROM addresses and verify that the contents are proper. No PROM's or blank PROM's should read FF. Look at addresses FE04-FE07 and FE08-FE0B which are the control and data registers of the PIA chips. The even addresses should read 00 and the least significant 6 bits of the odd addresses should also be zero. Look also at FE00 which should contain 00. This is the control register of the ACIA chip. The data register at FE01 may contain anything but it should be steady.

If all is well at this point the test program supplied with the K-1012 should be loaded through the keyboard and dumped to cassette tape. The entry point is 0200 and the program should return to the monitor shortly thereafter. If memory location 0000 contains 00, the diagnostic ran without error. Otherwise an error code has been stored and the program listing should be consulted to interpret the error. Then the troubleshooting guide elsewhere in this manual should be consulted for a possible solution.

I/O BASE ADDRESS STRAPPING

BASE ADDRESS	JUMPER THESE PINS TOGETHER			
* 00	U10-1 & 16	U10-3 & 14	U10-5 & 12	U10-7 & 10
10	U10-1 & 16	U10-3 & 14	U10-5 & 12	U10-8 & 9
20	U10-1 & 16	U10-3 & 14	U10-6 & 11	U10-7 & 10
30	U10-1 & 16	U10-3 & 14	U10-6 & 11	U10-8 & 9
40	U10-1 & 16	U10-4 & 13	U10-5 & 12	U10-7 & 10
50	U10-1 & 16	U10-4 & 13	U10-5 & 12	U10-8 & 9
60	U10-1 & 16	U10-4 & 13	U10-6 & 11	U10-7 & 10
70	U10-1 & 16	U10-4 & 13	U10-6 & 11	U10-8 & 9
80	U10-2 & 15	U10-3 & 14	U10-5 & 12	U10-7 & 10
90	U10-2 & 15	U10-3 & 14	U10-5 & 12	U10-8 & 9
A0	U10-2 & 15	U10-3 & 14	U10-6 & 11	U10-7 & 10
B0	U10-2 & 15	U10-3 & 14	U10-6 & 11	U10-8 & 9
C0	U10-2 & 15	U10-4 & 13	U10-5 & 12	U10-7 & 10
D0	U10-2 & 15	U10-4 & 13	U10-5 & 12	U10-8 & 9
E0	U10-2 & 15	U10-4 & 13	U10-6 & 11	U10-7 & 10
F0	U10-2 & 15	U10-4 & 13	U10-6 & 11	U10-8 & 9

PIA 1: FUNCTION	JUMPER TOGETHER
Enable IRQ A	U36-5 & 12
Enable IRQ B	U36-7 & 10
* CB1 to A-21	U36-4 & 13
* CB2 to A-22	U36-2 & 15

PIA 2:	
Enable IRQ A	U36-6 & 11
Enable IRQ B	U36-8 & 9

ACIA	
Carrier Detect from A-21	U36-3 & 14
Clear To Send from A-22	U36-1 & 16

BAUD RATE: (Be sure to select divide by 16 mode in ACIA)

75	U41-3 & 14	U41-1 & 16
110	U41-3 & 14	
150	U41-4 & 13	U41-1 & 16
* 300	U41-8 & 9	U41-1 & 16
600	U41-7 & 10	U41-1 & 16
1200	U41-6 & 11	U41-1 & 16
2400	U41-5 & 12	U41-1 & 16
4800	U41-2 & 15	U41-1 & 16

* = Standard jumper supplied with assembled board.

HOW TO USE THE AUXILIARY PROM BLOCK

The auxiliary PROM block was included to hold utility software such as I/O routines after the main PROM block is filled with BASIC or an assembler. It essentially works like the main PROM block except that only 4 PROM sockets are on the board. These 4 PROM's may be placed anywhere in the 8K block of addresses defined by the auxiliary PROM base address jumpers listed on a previous page. In the table below, inserting a jumper will activate an auxiliary PROM socket and enable the bus drivers on the board to drive the bus when the socket is selected. If no jumpers are inserted, none of the auxiliary PROM sockets will be activated and the bus drivers will not be activated for any of the addresses in the auxiliary block. The standard jumper configuration assigns the 4 PROMS to the lower half of the 8K block defined by the auxiliary PROM address jumpers.

ADDRESS RANGE (Offset from AUX base address)	STANDARD JUMPERS SHOWN		NAME	SOCKET
0000 - 03FF	U4-16	U4-1	AUX 0	U32
0400 - 07FF	U4-15	U4-2		
0800 - 0BFF	U4-14	U4-3	AUX 1	U33
0C00 - 0FFF	U4-13	U4-4		
1000 - 13FF	U4-12	U4-5	AUX 2	U30
1400 - 17FF	U4-11	U4-6		
1800 - 1BFF	U4-10	U4-7	AUX 3	U31
1C00 - 1FFF	U4-9	U4-8		

CONVERSION FROM 2708 PROMS TO TMS-2716 (Multi-voltage type)

For the convenience of our customers and to insure a longer life for the product, the K-1012 offers the capability to use 16K EPROM's which hold 2K bytes each. Because of the wide availability and low cost of 2708 EPROM's however most users would want to use them. Thus the jumpers required for 2708 operation have been wired-in. Conversion to TMS2716 may be accomplished by cutting the 2708 traces and soldering in jumper wires as listed below. The main and auxiliary arrays may be independently converted, but mixing of PROM's within the same array is not recommended. Note that when an array is converted that a 16K block of addresses is used and each PROM is worth 2K bytes.

To Convert the Main PROM Array to TMS2716

1. Remove jumper between U11-2 & U11-15
2. Solder in J7
3. If more than 4 TMS2716 are to be used, remove jumper from U12-13 or U12-14 and install a jumper from U12-14 to U12-11 or U12-12 whichever is open.
4. Cut the following traces on the PCB: J8,J9,J12,J13,J16,J17,J20,J21, J32,J33,J36,J37,J40,J41,J44,J45
5. Solder in the following jumpers: J10,J11,J14,J15,J18,J19,J22,J23 J34,J35,J38,J39,J42,J43,J46,J47

To Convert the Auxiliary PROM Array to TMS2716

1. Remove jumper between U11-1 & U11-16
2. Solder in J6
3. Cut the following traces on the PCB: J24,J25,J28,J29,J48,J49,J52,J53
4. Solder in the following jumpers: J26,J27,J30,J31,J50,J51,J54,J55

To Convert the PROM Programmer to TMS2716 (Be sure to read PROM programmer theory of operation after making this change)

1. Cut the following traces on the PCB: J1,J4
2. Solder in the following jumpers: J2,J3,J5

SPECIFICATIONS

PROM Capacity - 12K using industry standard 2708, 24K using TMS2716 (multivoltage)

Parallel I/O - Four 8-bit ports and 8 handshaking lines, each bit of each port may be programmed as an input or an output. Interrupt available for each group of 8 bits. 6520 PIA chips are used.

Serial I/O - - Asynchronous, 5-8 data bits; even, odd, or no parity; 1 or 2 stop bits. RTS, CTS, and CD modem control signals are provided. Baud rates of 75, 110, 150, 300, 600, 1200, 2400, 4800 are provided with an accuracy of .2% or better with a 1mHz system clock. Serial data and modem signals are true RS-232 levels. A 6850 ACIA chip is used.

PROM Programmer Can program standard 2708 EPROMS or with a jumper change, TMS2716

Access Time - - 550NS maximum as required by KIM-1 when using 450NS PROM's

Power Requirement - +7.5 volts unregulated .35 amp, +16 volts unregulated .25 amp. +26 and -5 voltages required by the PROM's are generated on-board.

Addressing - - 8K of PROM must be contiguous on an 8K boundary, remaining 4K may be scattered in a second 8K block. I/O requires 16 contiguous addresses which can be placed anywhere in the last or next-to-last page of any 4K block of addresses. IC sockets provided for all address jumpers.

Buffering - - - Buffering for both address and data busses is provided. Maximum bus load is 1 LS TTL gate input and one LS TTL tri-state output.

Physical Size - 7.5" X 11" exclusive of edge fingers. Two sets of 44 edge fingers compatible with the KIM-1, SYM-1, or AIM-65 processors.

PIN CONNECTIONS

EXPANSION CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
E-1	N.C.	E-A	ADDR BUS 0
E-2	N.C.	E-B	ADDR BUS 1
E-3	N.C.	E-C	ADDR BUS 2
E-4	INT. REQ.	E-D	ADDR BUS 3
E-5	N.C.	E-E	ADDR BUS 4
E-6	N.C.	E-F	ADDR BUS 5
E-7	RESET	E-H	ADDR BUS 6
E-8	DATA BUS 7	E-J	ADDR BUS 7
E-9	DATA BUS 6	E-K	ADDR BUS 8
E-10	DATA BUS 5	E-L	ADDR BUS 9
E-11	DATA BUS 4	E-M	ADDR BUS 10
E-12	DATA BUS 3	E-N	ADDR BUS 11
E-13	DATA BUS 2	E-P	ADDR BUS 12
E-14	DATA BUS 1	E-R	ADDR BUS 13
E-15	DATA BUS 0	E-S	ADDR BUS 14
E-16	N.C.	E-T	ADDR BUS 15
E-17	N.C.	E-U	N.C.
E-18	+7.5 VOLTS IN	E-V	READ/WRITE
E-19	VECTOR FETCH	E-W	N.C.
E-20	DECODE ENABLE	E-X	+16 VOLTS IN
E-21	N.C.	E-Y	PHASE 2
E-22	GROUND	E-Z	N.C.

APPLICATION CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
A-1	GROUND	A-A	SERIAL DATA IN
A-2	EIA RTS	A-B	SERIAL DATA OUT
A-3	PIA 2 CA1	A-C	PIA 1 CA1
A-4	PIA 2 CA2	A-D	PIA 1 CA2
A-5	PIA 1 PA0	A-E	PIA 2 PA0
A-6	PIA 1 PA1	A-F	PIA 2 PA1
A-7	PIA 1 PA2	A-H	PIA 2 PA2
A-8	PIA 1 PA3	A-J	PIA 2 PA3
A-9	PIA 1 PA4	A-K	PIA 2 PA4
A-10	PIA 1 PA5	A-L	PIA 2 PA5
A-11	PIA 1 PA6	A-M	PIA 2 PA6
A-12	PIA 1 PA7	A-N	PIA 2 PA7
A-13	PIA 1 PB0	A-P	PIA 2 PB0
A-14	PIA 1 PB1	A-R	PIA 2 PB1
A-15	PIA 1 PB2	A-S	PIA 2 PB2
A-16	PIA 1 PB3	A-T	PIA 2 PB3
A-17	PIA 1 PB4	A-U	PIA 2 PB4
A-18	PIA 1 PB5	A-V	PIA 2 PB5
A-19	PIA 1 PB6	A-W	PIA 2 PB6
A-20	PIA 1 PB7	A-X	PIA 2 PB7
A-21	(note 1)	A-Y	PIA 2 CB1
A-22	(note 2)	A-Z	PIA 2 CB2

Note 1: A jumper selects between EIA CD and PIA 1 CB2 (PIA 1 CB2 is standard)

Note 2: A jumper selects between EIA CTS and PIA 1 CB1 (PIA 1 CB1 is standard)

PRINCIPLES OF OPERATION

Although the K-1012 PROM/IO board is large and has a lot of components, its design and operation are relatively simple. Looking at the block diagram the board is seen to consist of a bus buffer, address decoder, main PROM block, auxiliary PROM block, parallel I/O block, serial I/O block, on-board power supply, and PROM programmer.

The address and data busses are buffered by the bus buffer block. The address buffer is simple since it is unidirectional but the data buffer must be bidirectional. In particular the data out drivers must only be activiated during read cycles to valid K-1012 addresses.

The address decoder establishes the range of memory addresses assigned to the two PROM blocks and the I/O blocks. Each of these three address ranges has its own independent address decoder. Another function of the address decoder is to provide the VECTOR FETCH and DECODE ENABLE signals needed by the KIM-1 when external memory is added. These signals serve no function with the SYM-1 and AIM-65 processors.

The main and auxiliary PROM blocks combined hold 12 PROMS; 8 in the main block and 4 in the auxiliary block. These blocks are independently enabled by their corresponding address decoder. The auxiliary PROM block, since it is not completely filled, feeds an enable signal back to the bus buffers only when a PROM actually responds to an address. Any addresses within the auxiliary block range that do not actually activate a PROM will not activate the data out drivers. Discrete circuitry within the two PROM blocks applies power to a PROM only when it is addressed thus drastically reducing power consumption.

The two I/O blocks are enabled by the address decoder when one of the 16 I/O addresses is referenced. Although there are only 10 unique I/O addresses, 16 are occupied (4 give undefined results and 2 are duplicated). The parallel I/O chips are just tied to the application edge fingers. The serial I/O chip's TTL levels are converted to/from EIA levels by discrete circuitry. All of the interrupt request signals from the I/O chips may be wire-ored together (via jumpers) and connected to the IRQ bus line. The baud rate generator for the serial port is implemented with a programmable counter driven by the system clock which is assumed to be crystal controlled at 1mHz.

The on-board power supply converts the +8 and +16 volt unregulated inputs to +5 and +12 volts regulated for the logic and PROM's. A charge pump circuit driven at the system clock frequency provides -5 volts regulated for the PROM's and an unregulated voltage of about 35 volts for the PROM programmer. The 35 volts is stored on a capacitor which then supplies the surge currents necessary during programming.

The PROM programmer is driven by part of the parallel I/O block. Eight bits are used to interface to the 8 data lines thus allowing the PROM to be read as well as programmed. Four additional bits are used to control the address counter and initiate program pulses. Although software determines the timing of the programming sequence, a fail-safe circuit protects the PROM from software crashes.

BUS BUFFERS AND ADDRESS DECODER

The majority of the bus interface circuitry is on page 2 of the detailed schematic drawings. Some of the 16 address lines are buffered by AND gates with the unused input tied high while those that must be available in true and complement form for the address decoder are run through two series inverters. All of these gates are low power Schottky to minimize bus loading whithout delaying the signals appreciably. U19, U20, and U21 are non-inverting tri-state buffers which are interconnected to form a bidirectional transceiver for the data bus. Both directions are disabled except during phase two of cycles that actually address something on the board. Again the LS version of these buffers is used to minimize bus loading and noise. The drive capability is fairly low which keeps switching noise down.

The mass of logic at the upper right of the diagram is the address decoder. U9-8 and U9-6 are the auxiliary and main PROM block detects respectively. Since either block of addresses is 8K and must be on an 8K boundary, only A13 - A15 needs to be considered. Jumpers in the U15 and U12 area select the desired combination of true and complement A13 - A15 lines for the desired address block. If TMS-2716 PROMS are being used in the main array and it is desired to increase the block size to 16K, then the A13 jumper should be omitted and U9-3 should be jumpered to U9-5.

The block of 16 addresses used by the I/O circuitry is detected in two stages. The first stage is the detection of the I/O page address. It is assumed that the user desires to have I/O registers throughout the system (excluding those that are part of the processor board) all reside in the same memory page which is tucked away in a corner away from mainstream memory. U8 is used to detect this I/O page. The connections to A9 - A11 are fixed as E or F (hexadecimal) but jumpers select the connections to A8 and A12 - A15. Thus the I/O page may be set to XE or XF where X is any hexadecimal digit. In KIM-1 systems X must be F if the VECTOR FETCH signal is to be used. In other systems X can be anything but the user must be careful to avoid interference with addresses on the processor board or other expansion boards or other portions of the K-1012 board. U7 implements the second stage of I/O address recognition. When enabled by U8 through inverter U5-3, it looks at A4 - A7 which can be jumpered in any combination of true and complement.

The DECODE ENABLE signal for the KIM-1 simply looks for A13 - A15 to be 000. When this combination is detected, the DECODE ENABLE line is driven low which then activates memory circuitry on-board the KIM-1. By convention VECTOR FETCH must be pulled low when one of the vector locations (FFFA-FFFF) is accessed by the processor. To simplify decoding circuitry, MTU boards broaden the range to include all addresses between FF00 to FFFF, i.e., page FF. Open-collector gate U2-3 in conjunction with the I/O page decoder detects page FF and pulls VECTOR FETCH down as required. For this to work properly, the I/O page must be set to FE or FF. If the KIM-1 user desires the I/O page elsewhere, U2-3 must be disconnected from the bus and the system must have either another MTU board installed or the user must provide for the VECTOR FETCH function. (Note: reset vectoring directly into PROM may be achieved in KIM systems by disconnecting the VECTOR FETCH signal from the processor and having PROM in the E000 - FFFF 8K block)

Further address decoding for the PROM's is accomplished on page 1 by decoders U1 and U3. Each decoder is activated by its respective PROM ARRAY ENABLE and looks at A10 - A12 to produce 8 mutually exclusive outputs which in turn enable particular PROM's. J6 and J7, which switches the decoder A input between A10 and A13, is used to convert between 2708 and TMS2716 PROM's. U4 is a jumper socket for the auxiliary PROM array. For every prom installed in this array, a jumper must be inserted to connect the PROM's chip enable to a decoder output.

BUS BUFFERS AND ADDRESS DECODER con't

Final address decoding for the two PIA chips and the ACIA chip is done with their multiple chip select inputs. The ACIA responds when A2 and A3 are both low thus it occupies the lowest 4 locations within the 16 I/O address block. PIA 1 responds when A2 is low and A3 is high and PIA 2 responds to the converse situation. Nothing responds when A2 and A3 are both high.

The function of U6 is to logical OR all of the enable signals generated by address decoding so that the data bus buffer is properly controlled. This OR function is then ANDed with Read/Write and Phase 2 so that the bus buffer is only activated during Phase 2 when the board is addressed. This is necessary to avoid noise from overlap of drive-in and drive-out buffer enable signals. Discrete diodes are used for this function on REV-A boards. Note that there is individual feedback from the auxiliary PROM block so that the bus is not driven when a non-existant auxiliary PROM is addressed.

PROM's

Connection to the PROM's is quite straightforward. Essentially they are chip selected by the address decoder and look at A0 - A9 for final addressing. The power-down circuit is unique however. When chip select goes down on a PROM, the PNP transistor in series with its +12 lead is turned on by base drive through the series 1K resistor and 9.1V zener diode. The zener diode provides logic level shifting so that a 3 volt logic signal can drive the base at +12 potential. It is important when deselecting a PROM that chip select go high a couple of hundred NS before power is removed; if this is not done, the PROM will remain selected and drive its outputs for several milliseconds until internal nodes discharge. This delay is provided by the storage time of the PN/2N2907 transistors used. If a substitution is made, gold doped high speed switches must be avoided. The small amount of leakage that occurs with no resistor between base and emitter is of no consequence. The bleeder resistor shown between emitter and collector is not normally installed on the board. A resistor in the 1K to 3K range can be installed if the PROM's have unusually slow power-up characteristics or a short circuit will bypass power switching altogether. If the power down circuit is bypassed, only 8 PROM's can be used without overloading the power supply circuits.

Parallel I/O

The parallel I/O circuitry is a model of simplicity. The three chip select inputs on the 6520 (identical to the Motorola 6820) PIA chips are used as the final level of address decoding and A0 and A1 are used to select among the 4 internal addresses. For PIA 2, all 20 of the peripheral lines are routed straight to edge fingers. Only 18 from PIA 1 are wired directly but the other two (CB1 and CB2) may be jumpered to edge fingers if modem control signals on the serial port are not needed. The interrupt request outputs from the PIA chips may be individually jumpered onto the IRQ bus line. These jumpers are left out of factory assembled units to avoid possible confusion of inexperienced programmers.

Note that port A of PIA 2 is connected to the PROM programmer socket. However if no PROM is plugged in, there is no load on these lines. PB0 through PB3 also go into the programmer circuitry. PB2 and PB3 are not loaded since they drive CMOS. PB1 is loaded by 1LS TTL load which is about 1/5 of its drive capability. PB0 however is loaded such that 1-to-0 transitions after being in the 1 state for a long time are likely to be slow. In any case, when programming PROM's all external connections to these lines should be removed.

Serial I/O

Serial I/O capability is provided by a 6850 ACIA chip. It is addressed like the PIA chips but only A0 is looked at since there are only two internal registers to select. The chip however provides and accepts TTL logic levels while standard serial interfaces accept and provide EIA logic levels which swing between -5 and +5 volts minimum. The transistor circuits using Q22 - Q24 translate such input levels to TTL for the PIA chip. These inputs will withstand up to ±30 volts but will also accept TTL level inputs. The 10K pullups on the carrier detect and clear-to-send inputs insure normal operation of the ACIA when these modem control signals are not used.

U39, which is a dual op-amp, provides very inexpensive and low power conversion from TTL levels to EIA levels. Essentially the op-amps are wired as comparators with a 2.5 volt threshold. The slew rate limit of the internally compensated amplifiers also provides a controlled rise and fall time of about 25 microsecond.

The baud rate generator consists of programmable counter U37 and post divider U38. U37 divides the 1mHz system clock by either 9 or 13 according to a jumper setting. In operation the counter is preset to 7 for divide by 9 or 3 for divide by 13. It then counts up at a 1mHz rate until it reaches 15. The next clock puise will preset it again through the terminal count output and U44-11. U38 is a simple ripple counter and jumpers tap off various frequencies for the ACIA.

Power Supply

The majority of the power supply is on page 2 of the schematic. Unregulated +8 and +16 volt inputs are regulated to +5 and +12 volts by VR3 and VR2 respectively. Each regulator has input capacitors to prevent oscillation and output capacitors to absorb large transient currents. The 1000uF input capacitor on the +16 volt line provides the additional filtering required when using our K-1000 series power supplies.

A charge pump circuit supplies negative and high positive voltages to the PROM's and PROM programmer. U2 and Q1 and Q2 provide a low impedance 12 volt square wave at the 1mHz system clock frequency. Pullup resistor R1 being returned to +16 volts insures adequate base drive to Q2 so that a full 12 volt swing is achieved even with heavy loads. D1, D2, C20, and C22 form a familiar half-wave voltage doubler circuit. The negative output voltage is achieved by returning D1's cathode to ground. C20 develops a charge of approximately -8 to -10 volts which then feeds VR1 to be regulated to -5 volts. C34 is a high frequency input bypass for VR1 which prevents oscillation.

On page 3 of the schematic is another charge pump circuit configured as a parallel voltage quadrupler. Its operation is similar to the negative power supply except that "common" is returned to +12 volts and there are two complete doubler stages. In operation C28 accumulates a charge of +35 volts which is used by the PROM programmer.

PROM PROGRAMMER

The PROM programmer is in the upper right corner of page 3. It consists of programming socket U34, address counter U35 and high voltage program pulse circuitry. The 8 data lines of U34 are tied directly to one of the parallel ports. Since the port may be set up for either input or output, the PROM may be both written and read without moving it out of the programming socket.

Address counter U35 provides sequential addressing of the 1024 locations in the PROM. The counter may be incremented and reset through 2 I/O port bits. This single chip CMOS counter saves considerable circuitry and tends to enforce sequential programming of the PROM in "passes" as recommended by the manufacturer.

The chip select input to the PROM requires special attention. For a 2708, +5 volts deselects the chip and ground selects it for reading. Positive 12 volts readies it for programming. Since the programming socket never needs to be deselected, this pin is driven between +12 and ground by U44-3. For a 2716, this pin is the 11th address pin so it is jumpered to the address counter instead. The write enable pin is the +5 supply to the chip. When reading, +5 volts is supplied by emitter follower Q16 which is saturated by the 12 volt drive of U44-3 and R37. When programming, this pin is solidly grounded by Q15, another emitter follower.

By far the most critical input to the PROM is the program pulse. This pulse must be +26 volts in amplitude to close tolerances and must be able to sink current when in the zero voltage state. Furthermore, the rise and fall times must be controlled and a current limit circuit should be included to prevent the PROM from drawing too much current during programming. The 5 transistor circuit using Q17 - Q22 has all of these properties. The Q17-Q18 combination is a current limited switch to the +35 volt power supply. A current limit threshold of about 20MA is reached when the voltage drop accross R34 reaches .6 volts. Q19 and Q20 form a similar current limited switch to ground. When Q21 is off, which is the normal situation, current through R33, R32, and R35 turns Q20 on to ground the program pin. There is insufficient voltage drop accross R33 in this situation to turn Q18 on. When Q21 is turned on for a program pulse, base current to Q20 is cut off and the three times greater current flow through R33 now turns Q18 on. C27 and the 20MA current limit provides a controlled voltage rise time of 1.2uS. The pulse amplitude is clamped at +26 volts by D15 and LED 1. Fall time is also controlled since Q20 is part of a current limited circuit. C29 and C30 limit how long Q21 can be continuously energized and therefore provide a fail-safe function. Programming pulses should be a maximum of 500uS in duration and separated with a rest period of at least 500uS.

K-1012-1 PROM ONLY

The K-1012-1 PROM only board is the same etch pattern as the K-1012 but with all circuitry not associated with reading PROM's removed. In particular the drive-in bus buffers, I/O address decoder, parallel and serial I/O chips, and all PROM programmer components have been removed. The customer may install some or all of these components if desired but should be aware that those portions of the board have not been tested in any way.

TROUBLESHOOTING

Factory assembled K-1012 boards have been carefully checked out and burned-in prior to shipment. However because of the scores of jumper options available, some of which involve PC trace cutting, it is impossible to test 100% of the board functions. Also since the customer supplies the PROM's, we have no control over their quality. If at all possible the customer should test the board as received with no jumper changes to avoid confusion.

In the event of trouble first give the board a throrough visual inspection. Unclipped excess component leads may have bent over and shorted during shipment. A poor solder connection might have opened during shipping vibration. Check that all of the standard jumpers are in place and not shorting against each other. It goes without saying that all connections between the processor board and the K-1012 should be checked. In particular a heavy ground lead (braid, large PC foil area, or #18 hookup wire) should be used and the bus wire lengths should not exceed 4 inches.

Following this the first area to check is the power supply. The incoming power should read a minimum of +8 and +15 volts with a voltmeter. If an oscilloscope is available, the negative peak of the ripple waveform must not drop below +7 and +14 volts. Next check the output of the positive regulators. If the heatsink is blazing hot and one of the regulated voltages is low or zero, suspect a short, possibly through a user supplied PROM. Check the -5 volt output. If it is low or zero and the regulator is even warm, suspect a short, again most likely through a user supplied PROM. If it is zero and the regulator is cold, the trouble is in the charge pump circuit. If the the PROM programmer does not function, check the +35 volt programming supply. When not programming it should be at least +32 volts.

Addressing problems can be tracked down by noting which addresses the board does respond to. With most processors and monitors, a non-existant address will read back the page number of the non-existant address (this is due to the operation sequence of indirect addressing). If it responds to too many addresses (for example, I/O can be addressed at two different places), then either an address selection jumper is missing or a PC trace is open. This problem would most likely occur after the jumpers had been reconfigured by the user.

Problems in reliably reading PROM's will probably be the most common since we have no control over their quality. In particular 450NS factory prime PROMS should be used. PROM's are not characterized for power down operation and therefore manufacturers do not guarentee the amount of time required to achieve normal operation after power up. However we have tested Motorola (MC2708L, MC68708), Intel, National Semiconductor, Signetics, and Texas Instruments for power down operation and found them to be satisfactory. Expect to pay $10 to $15 for good 2708 PROM's. Remember, the $7 bargain device might be someone else's reject because of slow power-up or out-of-spec access time.

Slow power-up is manifested by intermittant program operation, particularly when an infrequently used routine is in another PROM and the program crashes when using that routine. The condition can be checked by temporarily placing a shorting jumper in the bleed resistor position of the suspect PROM. If this cures the problem, then the PROM is probably slow to power up. Next try a 2.2K trickle resistor which will keep the PROM partially powered all the time and thereby reduce its power-up delay. If this fails too, try 1K. If still no luck, either leave the short in place or consider using a different PROM. If more than 4 shorting jumpers are used, there will be insufficient power to program PROMS unless the board is depopulated.

Programming PROM's should be done with the routine in the back of this manual. This program conforms exactly to the manufacturer's specifications and should program the PROM's thoroughly. Most programming problems are caused by incomplete erasure. PROM's being erased should be rotated once during erasure to overcome the effects of possible shadows from scratches or bits of label on the window.

If the customer cannot find the problem or is unable to repair it, return the board to the factory for repair, preferably with the customer's PROM's in place.

I/O PROGRAMMING TECHNIQUES

Both the parallel and the serial ports on the K-1012 use standard MOS interface chips. Full details about their operation and programming techniques is given in the manufacturer's specification sheets which are reproduced elsewhere in this manual. However several tips about their operation can be given here to get the user "up and running" quickly with a minimum of study.

PARALLEL PORTS

The two 6520 PIA chips provide 4 independent 8 bit ports plus 8 control lines. Each line of each port may be independently programmed for input or output although most applications would not mix functions on the same 8 bit port. Ports to be used as outputs must first be set up as outputs by writing all 1's into a special direction register. The 6520 does not address the direction register like the 6530 chips used on the KIM-1 or the 6522 chips used on the SYM-1 or AIM-65. Instead the direction registers share the same address as the data register. Selection between direction and data register addressing is controlled by bit 2 in the control register associated with each port. If bit 2 is a zero, the direction register is selected and if it is a one, the data register is selected. Thus initialization of a port for output would be accomplished by writing $00 to the control register, writing $FF to the direction/data register, and then writing $04 to the control register. The port is now set up as an output and all of the extra functions of the 6520 are disabled. For inputs, it is only necessary to write $04 to the control register; power up reset has already set the data direction register to zero. Like most MOS interface chips the contents of the data register may be read back thus allowing shifts and increment/decrement directly in the I/O register. However if the port A outputs are heavily loaded (such as by directly tying to transistor bases), the port cannot be read back accurately. Port B is buffered to prevent this problem.

The 6520 has many other functions available which allow very flexible control of the two control lines and interrupt request for each port. Consult the data sheet for detailed programming information.

FUNCTION	ADDRESS	FUNCTION	ADDRESS
PIA 1 port A data/direction	FE04	PIA 2 port A data/direction	FE08
PIA 1 port A control	FE05	PIA 2 port A control	FE09
PIA 1 port B data/direction	FE06	PIA 2 port B data/direction	FE0A
PIA 1 port B control	FE07	PIA 2 port B control	FE0B

(NOTE: PIA 2 drives the programmer)

SERIAL PORT

Full operation of the serial port is much simpler than the parallel ports. Only two addresses and 4 registers are involved. Address FE01 when written to is the transmit data register and when read is the receive data register. Address FE00 when written to is the control register and when read is the status register.

The first step in using the serial port is to set up the various transmission parameters. The standard setting is $11 which gives 8 data bits, 2 stop bits, no parity, 16X clock, and interrupts disabled. Before writing this into the control register, a $03 byte must be written to reset the chip. After configuration, bit 0 in the status register goes to a 1 when a data byte is received and goes back to zero when the receive data register is read. To transmit a byte it must be stored in the transmit data register. Bit 1 in the status register will then be set when the byte has been transmitted and another can be stored. The act of storing into the transmit data register will reset this bit.

The 6850 is also capable of numerous combinations of data bit count, parity generation/checking, 1X and 64X clock dividers, and independent receive and transmit interrupts. To use these functions effectively, consult the data sheet.

PROM PROGRAMMER OPERATION

The easiest way to use the PROM programmer on the K-1012 is to use the PROM programmer program listed in the back of this manual. The K-1012 is shipped with an ordinary but high quality 24 pin programming socket. If the board is to be used for extensive programming (over 100 PROM's), a zero-insertion-force socket (Textool equivalent) wired to a short cable with 24 pin DIP plug and inserted into the programming socket is recommended.

1. Be sure the PROM is thoroughly erased. Germacidal or ozone lamps generally require 30 minutes (longer if the lamp is old) with the PROM placed 1 inch from the arc. New PROM's should be erased since their history is unknown.

2. Disconnect any peripheral devices connected to PIA 2 port A or bits 0-3 of port B that may be disturbed by random signals or which significantly load these lines.

3. Load the data to be programmed into RAM somewhere other than pages 0-3. Remember that all 1024 locations of the 2708 must be programmed at once; partial programming is not possible or safe for the PROM. Also note that the data need not reside at the same addresses that it will when the programmed PROM's are installed on the K-1012.

4. Load the PROM programmer program into RAM from the listing. If the 16 I/O addresses assigned to the K-1012 are not FE00 - FE0F, see the program listing for the necessary changes. The changes necessary for programming 2704's and TMS2716's are also shown in the listing.

5. Set locations 0004 (L) and 0005 (H) to the RAM address containing the data to program.

6. With the program enable switch in the OFF position, insert the blank PROM into the programming socket. It is safe to do this with the power on. If the environment is dry, discharge your body to ground before plugging the PROM in.

7. Verify that the PROM is blank by executing NEWPRM (0200). Location 0000 will read FF if the PROM is indeed blank otherwise it will contain the contents of the first non-blank cell and locations 0002 (L) and 0003 (H) will contain the RAM address of the corresponding non-blank location in the PROM.

8. Turn the program enable switch ON. DO NOT PRESS RESET WHILE THE SWITCH IS ON OR FALSE DATA MAY BE PROGRAMMED INTO THE PROM!

9. Execute PGMVFY (0203) to actually program the PROM. The program pulse LED should light during programming. Programming will require about 4 minutes after which the monitor should be re-entered. The PROM contents are compared against RAM after programming is complete. If this verify is successful, locations 0000 - 0003 will be 00. If not, location 0000 will contain the data actually in the PROM, location 0001 will contain the data that should have been in the PROM, and locations 0002 (low) and 0003 (high) will contain the RAM address of the data that did not program correctly.

10. Turn the program enable switch OFF. If the PROM verified, set aside for use later. If it did not verify write a question mark on it and restock unless it already has a question mark in which case it should be discarded or returned to the seller.

An unknown PROM may be compared against RAM contents by following steps 2-6 and then entering VERIFY (0206). This is the same routine that is executed after a programming cycle and it signals errors in the same manner.

A PROM may be copied by first reading it into RAM with READ (0209). Set up the RAM address in 0004 and 0005 and go to READ (0209). The original PROM may now be removed and a blank one installed. Follow the programming proceedure outlined above to program the copy PROM. There is no danger of damaging the original PROM as long as the program enable switch is off.

PROGRAMMING PROM'S ON A SYM-1

In order to use the PROM programming program on a SYM all references to I/O port addresses will have to be changed since it will not be possible to set the I/O page address to FE in a SYM system. All I/O port references are marked with ****'s in the program listing. Also the return jump to the monitor in location 020C will have to be changed to 4C to return to the SYM-1 monitor. These are the only changes necessary as there are no monitor calls in the program and page zero usage is minimal.

PROGRAMMING PROM'S ON AN AIM-65

In order to use the PROM programming program on an AIM all references to I/O port addresses will have to be changed since it will not be possible to set the I/O page address to FE in an AIM system. All I/O port references are marked with ****'s in the program listing. Also the return jump to the monitor in location 020C will have to be changed to 4C BF E0 to return to the AIM-65 monitor. These are the only changes necessary as there are no monitor calls in the program and page zero usage is minimal.

APPLICATION INFORMATION

INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

REGISTER ADDRESSING

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 – INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. All Data Direction Register bits set at "0" configure the corresponding peripheral data line as an input; all "1s" result in an output.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

TABLE 2 – CONTROL WORD FORMAT

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

Data Direction Access Control Bit (CRA-2 and CRB-2) – Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) – The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

TABLE 3 – CONTROL OF INTERRUPT INPUTS CA1 AND CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled – $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled – $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

NOTES: 1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs on the positive transition of CRA-0 (CRB-0).

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

TABLE 4 – CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS
CRA5 (CRB5) is low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled – $\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled – $\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high

NOTES: 1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs on the positive transition of CRA-3 (CRB-3).

TABLE 5 – CONTROL OF CA2 AS AN OUTPUT
CRA-5 is high

CRA-5	CRA-4	CRA-3	CA2 Cleared	CA2 Set
1	0	0	Low on negative transition of E after an MPU Read "A" Data operation.	High on an active transition of the CA1 signal
1	0	1	Low immediately after an MPU Read "A" Data operation.	High on the negative edge of the next "E" pulse
1	1	0	Low when CRA-3 goes low as a result of an MPU Write in Control Register "A".	Always low as long as CRA-3 is low.
1	1	1	Always high as long as CRA-3 is high	High when CRA-3 goes high as a result of a Write in Control Register "A".

TABLE 6 – CONTROL OF CB2 AS AN OUTPUT
CRB-5 is high

CRB-5	CRB-4	CRB-3	CB2 Cleared	CB2 Set
1	0	0	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal
1	0	1	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High on the positive transition of the next "E" pulse.
1	1	0	Low when CRB-3 goes low as a result of an MPU Write in Control Register "B".	Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register "B" that changes CRB-3 to "one".
1	1	1	Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to "zero".	High when CRB-3 goes high as a result of an MPU write into control register "B".

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) – The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Status lines when those lines are programmed to be interrupt inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

APPLICATION INFORMATION

INTERNAL REGISTERS–The ACIA has four internal registers utilized for status, control, receiving data, and transmitting data. The register addressing by the R/W and RS lines and the bit definitions for each register are shown in Figure 4.

FIGURE 4 – DEFINITION OF ACIA REGISTERS

	BUFFER ADDRESS			
	RS • $\overline{R/W}$	RS • R/W	$\overline{RS}$ • $\overline{R/W}$	$\overline{RS}$ • R/W
Data Bus Line Number	Transmit Data Register	Receiver Date Register	Control Register	Status Register
	(Write Only)	(Read Only)	(Write Only)	(Read Only)
0	Data Bit 0*	Data Bit 0*	Clk. Divide Sel. (CR0)	Rx Data Reg. Full (RDRF)
1	Data Bit 1	Data Bit 1	Clk. Divide Sel. (CR1)	Tx Data Reg. Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Sel. 1 (CR2)	Data Carrier Det. loss ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Sel. 2 (CR3)	Clear-to-Send (CTS)
4	Data Bit 4	Data Bit 4	Word Sel. 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Tx Control 1 (CR5)	Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Tx Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Rx Interrupt Enable (CR7)	Interrupt Request (IRQ)

Notes:
* Leading bit = LSB = Bit 0
** Unused data bits in received character will be "0's."
*** Unused data bits for transmission are "don't care's."

ACIA STATUS REGISTER—Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This Read Only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of: transmitting data register, the receiving data register and error status and the modem status inputs of the ACIA.

Receiver Data Register Full (RDRF) [Bit 0] – Receiver Data Register Full indicates that received data has been transferred to the Receiver Data Register. RDRF is cleared after an MPU read of the Receiver Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receiver Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE) [Bit 1]—The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$) [Bit 2] – The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated if the Receiver Interrupt Enable (RIE) is set. It remains high until the interrupt is cleared by reading the Status Register and the data register or a Master Reset occurs. If the $\overline{DCD}$ input remains high after Read Status and Read Data or Master Reset have occurred, the $\overline{DCD}$ Status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$) [Bit 3] – The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master Reset does not affect the Clear-to-Send status bit.

Framing Error (FE) [Bit 4] – Framing error indicates that the received character is improperly framed by the start and stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receiver data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN) [Bit 5] – Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receiver Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until Overrun is reset. Character synchronization is maintained during the Overrun condition. The overrun indication is reset after the reading of data from the Receive Data Register. Overrun is also reset by the Master Reset.

Parity Error (PE) [Bit 6]—The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$) [Bit 7]—The IRQ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt that is set and enabled will be indicated in the status register. Any time the $\overline{IRQ}$ output is low the IRQ bit will be high to indicate the interrupt or service request status.

CONTROL REGISTER—The ACIA control Register consists of eight bits of write only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send modem control output.

Counter Divide Select Bits (CR0 and CR1) – The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a Master Reset for the ACIA which clears the Status Register and initializes both the receiver and transmitter. Note that after a power-on or a power-fail restart, these bits must be set High to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷ 1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4)–The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bit
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not double-buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6)–Two Transmitter Control bits provide for the control of the Transmitter Buffer Empty interrupt output, the Request-to-Send output and the transmission of a BREAK level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled
1	1	$\overline{RTS}$ = low, Transmitting Interrupt Disabled and Transmits a BREAK level on the Transmit Data Output.

Receiver Interrupt Enable Bit (RIE) (CR7)–Interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Interrupts caused by the Receiver Data Register Full being high or by a low to high transition on the Data Carrier Detect signal line are enabled or disabled by the Receiver Interrupt Enable Bit.

TRANSMIT DATA REGISTER (TDR)–Data is written in the Transmit Data Register *during* the peripheral enable time (E) when the ACIA has been addressed and RS • R/$\overline{W}$ is selected. Writing data into the register causes the Transmit Data Register Empty bit in the status register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)–Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receiver Data Register Full bit (RDRF) (in the status buffer) to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receiver Data Register with RS and R/$\overline{W}$ high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receiver Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

OPERATIONAL DESCRIPTION

From the MPU Bus interface the ACIA appears as two addressable RAM memory locations. Internally, there are four registers; two read-only and two write-only registers. The read-only registers are status and receive data, and the write only registers are control and transmit data. The serial interface consists of serial transmit and receive lines and three modem/peripheral control lines.

During a power-on sequence, the ACIA is internally latched in a reset condition to prevent erroneous output transitions. This power-on reset latch can only be released by the master reset function via the control register; bits b_0 and b_1 are set "high" for a master reset. After master resetting the ACIA, the programmable control register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none) and etc.

TRANSMITTER–A typical transmitting sequence consists of reading the ACIA status register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmitter Data Register if the status read operation has indicated that the Transmit Data

Register is empty. This character is transferred to a shift register where it is serialized and transmitted from the Tx Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the data register, the status register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted. This second character will be automatically transferred into the shift register when the first character transmission is completed. The above sequence continues until all the characters have been transmitted.

RECEIVER–Data is received from a peripheral by means of the Rx Data input. A divide by one clock ratio is provided for an externally synchronized clock (to its data) while the divide by 16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide by 16 and 64 modes is obtained by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the status register along with framing error, overrun error, and receiver data register full. In a typical receiving sequence, the status register is read to determine if a character has been received from a peripheral. If the receiver data register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. The status register can be read again to determine if another character is available in the receiver data register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

```
                                .PAGE  'EQUATES AND DATA STORAGE'
  3                     ;       TEST AND EXERCISE PROGRAM FOR THE K-1012 ROM/IO BOARD.
  4                     ;       THIS IS A SIMPLIFIED TEST THAT DOES NOT REQUIRE A LOOP-AROUND
  5                     ;       PLUG ON THE APPLICATION CONNECTOR TO PERFORM.
  6                     ;       IT TESTS THE THREE I/O CHIPS FOR GROSS FUNCTION.
  7                     ;       EACH OF THE 4 REGISTERS IN EACH 6520 PIA CHIP IS TESTED FOR ITS
  8                     ;       ABILITY TO STORE 1'S AND ZEROES AND FOR MUTUAL NON-INTERFERENCE
  9                     ;       AMONG THE DATA REGISTERS, DIRECTION REGISTERS, AND CONTROL
 10                     ;       REGISTERS.
 11                     ;       THE TRANSMITTER IS TESTED FOR PROPER TRANSMISSION SPEED (300
 12                     ;       BAUD IS ASSUMED).
 13
 14                     ;       THE OVERALL TEST IS BROKEN DOWN INTO A NUMBER OF TESTS.  IF
 15                     ;       AN ERROR IS DETECTED, THE TEST NUMBER WILL BE STORED INTO
 16                     ;       LOCATION 0000.  AN ERROR CODE WILL BE STORED INTO LOCATION 0001
 17                     ;       FOR THOSE TESTS THAT HAVE MULTIPLE ERROR CONDITIONS.  LOCATION
 18                     ;       0002 WILL CONTAIN THE REGISTER ADDRESS THAT WAS BEING USED WHEN
 19                     ;       THE ERROR OCCURED.  LOCATION 0003 (LOW) AND 0004 (HIGH) SHOULD
 20                     ;       BE SET TO THE I/O BASE ADDRESS FOR THE BOARD.  BEFORE RUNNING
 21                     ;       THE DIAGNOSTIC
 22
 23                     ;                               TEST NUMBERS
 24                     ;       0  TEST PASSED
 25                     ;       1  MUTUAL INTERFERENCE TEST, FAILURE INDICATES A PROBLEM WITH
 26                     ;          ADDRESSING THE I/O REGISTERS SUCH AS SHORTED OR OPEN A1-A3.
 27                     ;       2  REGISTER DATA RETENTION TEST, FAILURE INDICATES A BAD I/O
 28                     ;          INTERFACE IC (SEE THE REGISTER ADDRESS TO DETERMINE WHICH
 29                     ;          IS BAD) OR AN OPEN OR SHORTED DATA LINE.
 30                     ;       3  ACIA TRANSMISSION SPEED TEST, FAILURE INDICATES FAILURE TO
 31                     ;          TRANSMIT OR INCORRECT TRANSMISSION SPEED (300 BAUD ASSUMED)
 32
 33                     ;       FOR SPECIFIC ERROR CODES, SEE THE PROGRAM LISTING
 34
 35                     ;                               REGISTER ADDRESSES
 36                     ;       0  ACIA (6850) CONTROL AND STATUS REGISTER
 37                     ;       1  ACIA (6850) DATA REGISTER
 38                     ;       4  PIA 2 PORT A DIRECTION AND DATA REGISTERS
 39                     ;       5  PIA 2 PORT A CONTROL REGISTER
 40                     ;       6  PIA 2 PORT B DIRECTION AND DATA REGISTERS
 41                     ;       7  PIA 2 PORT B CONTROL REGISTER
 42                     ;       8  PIA 1 PORT A DIRECTION AND DATA REGISTERS
 43                     ;       9  PIA 1 PORT A CONTROL REGISTER
 44                     ;       A  PIA 1 PORT B DIRECTION AND DATA REGISTERS
 45                     ;       B  PIA 1 PORT B CONTROL REGISTER
 46
 47
 48                     ;       KIM SYSTEM EQUATES
 49
 50 1C22        KIMMON  =       X'1C22          ; ADDRESS OF SAVE MACHINE STATE ENTRY POINT
 51
 52                     ;       BASE PAGE DATA STORAGE
 53 0000                .=      0
 54
 55 0000 00     TSTNO:  .BYTE   0               ; TEST IN ERROR, ZERO IS OK
 56 0001 00     ERRNO:  .BYTE   0               ; SPECIFIC FAILURE ERROR CODE
 57 0002 00     REGAD:  .BYTE   0               ; RELATIVE REGISTER ADDRESS ASSOCIATED
 58                                             ; WITH THE ERROR
 59 0003 00FE   IOBASE: .WORD   X'FE00          ; BASE ADDRESS OF I/O SECTION, FE00 IS
 60                                             ; STANDARD ON KIM SYSTEMS
 61
```

```
                                .PAGE  'TEST 1 - MUTUAL INTERFERENCE TEST'
 62                     ;       TEST 1 - MUTUAL INTERFERENCE TEST
 63                     ;       STORE A DIFFERENT PATTERN IN EACH OF THE REGISTERS AND THEN GO
 64                     ;       BACK AND VERIFY THAT THE PATTERNS REMAINED.  SOME OF THE
 65                     ;       PATTERNS MUST BE CAREFULLY CHOSEN TO AVOID UNUSUAL CONTROL
 66                     ;       FUNCTIONS.
 67
 68 0005                        .=      X'0200          ; START CODE AT 200
 69 0200 D8             TEST1:  CLD                     ; KILL DECIMAL MODE
 70 0201 A200                   LDX     #0              ; INITIALIZE TABLE INDEX
 71 0203 BC3102         TEST1A: LDY     ADTAB1,X        ; PICK UP REGISTER ADDRESS
 72 0206 BD3902                 LDA     DATAB1,X        ; PICK UP REGISTER DATA
 73 0209 9103                   STA     (IOBASE),Y      ; STORE SPECIFIED DATA INTO SPECIFIED ADDR
 74 020B E8                     INX                     ; INCREMENT INDEX
 75 020C E008                   CPX     #8              ; TEST IF ALL DONE
 76 020E D0F3                   BNE     TEST1A          ; LOOP IF NOT
 77
 78 0210 A200                   LDX     #0              ; REINITIALIZE TABLE INDEX FOR VERIFY PHASE
 79 0212 BC3102         TEST1B: LDY     ADTAB1,X        ; PICK UP REGISTER ADDRESS
 80 0215 B103                   LDA     (IOBASE),Y      ; GET THE REGISTER DATA BACK
 81 0217 293F                   AND     #X'3F           ; IGNORE TWO MOST SIGNIFICANT BITS =
 82                                                     ; INTERRUPT REQUEST IN CONTROL REGISTERS
 83 0219 DD3902                 CMP     DATAB1,X        ; COMPARE WITH DATA THAT WAS WRITTEN
 84 021C D008                   BNE     TEST1C          ; JUMP OUT IF WRONG
 85 021E E8                     INX                     ; INCREMENT INDEX
 86 021F E008                   CPX     #8              ; TEST IF ALL DONE (NOTE THAT ACIA
 87                                                     ; REGISTERS CANNOT BE READ BACK)
 88 0221 D0EF                   BNE     TEST1B          ; LOOP IF NOT
 89 0223 4C4102                 JMP     TEST2           ; GO TO NEXT TEST IF OK
 90                                                     ; DISTINCTION BETWEEN DATA REGISTERS AND
 91                                                     ; DATA DIRECTION REGISTERS WILL BE TESTED
 92                                                     ; IN TEST 2
 93
 94 0226 8402           TEST1C: STY     REGAD           ; LOG THE ERROR
 95 0228 A901                   LDA     #1              ; TEST 1
 96 022A 8500                   STA     TSTNO
 97 022C 8501                   STA     ERRNO           ; ERROR NUMBER 1
 98 022E 4CF702                 JMP     ETEST           ; RETURN TO MONITOR
 99
100 0231 09080B0A       ADTAB1: .BYTE   9,8,X'B,X'A             ; ADDRESS TABLE
101 0235 05040706               .BYTE   5,4,7,6
102 0239 20012802       DATAB1: .BYTE   X'20,X'01,X'28,X'02     ; DATA PATTERN TABLE
103 023D 30043808               .BYTE   X'30,X'04,X'38,X'08
104
```

TEST 2 -- DATA RETENTION TEST

```
                                .PAGE  'TEST 2 - DATA RETENTION TEST'
105                     ;       DATA RETENTION TEST
106                     ;       TAKES EACH OF THE 8 PIA REGISTERS AND VERIFIES THAT ALL 256
107                     ;       POSSIBLE BIT PATTERNS CAN BE STORED
108                     ;       INTERRUPT ENABLE JUMPERS FOR THE PIA'S SHOULD NOT BE INSTALLED
109
110 0241 A004       TEST2:  LDY     #4              ; SET ADDRESS OFFSET
111 0243 A900       TEST2A: LDA     #0              ; SELECT DIRECTION REGISTER IN PIA
112 0245 C8                 INY
113 0246 9103               STA     (IOBASE),Y
114 0248 88                 DEY
115 0249 207102             JSR     CYCLE           ; CYCLE THROUGH THE DATA PATTERNS IN THE
116                                                 ; DIRECTION REGISTER
117 024C A901               LDA     #1              ; ERROR NUMBER 1 FOR DIRECTION REGISTER
118 024E B016               BCS     TEST2B          ; JUMP OUT IF ERROR
119 0250 A904               LDA     #X'04           ; SELECT DATA REGISTER IN PIA
120 0252 C8                 INY
121 0253 9103               STA     (IOBASE),Y
122 0255 88                 DEY
123 0256 207102             JSR     CYCLE           ; CYCLE THE DATA REGISTER
124 0259 A902               LDA     #2              ; ERROR NUMBER 2 FOR DATA REGISTER
125 025B B009               BCS     TEST2B          ; JUMP OUT IF ERROR
126 025D C8                 INY                     ; SETUP TO GO TO THE NEXT PIA REGISTER PAIR
127 025E C8                 INY
128 025F C008               CPY     #8
129 0261 D0E0               BNE     TEST2A          ; LOOP UNTIL 4 REGISTER PAIRS TESTED
130 0263 4C8302             JMP     TEST3           ; GO TO NEXT TEST IF DONE
131
132 0266 8402       TEST2B: STY     REGAD           ; LOG THE ERROR, REGISTER ADDRESS
133 0268 8501               STA     ERRNO           ; ERROR NUMBER
134 026A A902               LDA     #2              ; TEST 2
135 026C 8500               STA     TSTNO
136 026E 4CF702             JMP     ETEST           ; RETURN TO MONITOR
137
138 0271 A200       CYCLE:  LDX     #0              ; CYCLE THROUGH REGISTER POINTED TO BY Y
139                                                 ; 256 TIMES
140 0273 8A         CYCLE1: TXA                     ; STORE DATA PATTERN
141 0274 9103               STA     (IOBASE),Y
142 0276 EA                 NOP
143 0277 EA                 NOP
144 0278 D103               CMP     (IOBASE),Y      ; RETRIEVE PATTERN AND TEST FOR VALIDITY
145 027A D005               BNE     CYCLE2          ; JUMP OUT IF DIFFERENT
146 027C E8                 INX                     ; TO NEXT PATTERN
147 027D D0F4               BNE     CYCLE1          ; LOOP IF NOT DONE
148 027F 18                 CLC                     ; CLEAR CARRY IF CYCLE WAS SUCCESSFUL
149 0280 60                 RTS                     ; AND RETURN
150 0281 38         CYCLE2: SEC                     ; SET CARRY IF CYCLE WAS NOT SUCCESSFUL
151 0282 60                 RTS                     ; AND RETURN
152
```

```
                                .PAGE  'TEST 3  TRANSMISSION SPEED TEST'
153                     ;       ACIA TRANSMISSION SPEED TEST
154                     ;       SINCE ALL OF THE ACIA REGISTERS ARE EITHER READ-ONLY OR WRITE-
155                     ;       ONLY IT IS NOT POSSIBLE TO TEST REGISTER FUNCTION WITHOUT A
156                     ;       LOOPAROUND CABLE.  THE TRANSMISSION SPEED CAN BE TESTED HOWEVER
157                     ;       WHICH GIVES REASONABLE ASSURANCE THAT THE 6850 CHIP IS
158                     ;       FUNCTIONING PROPERLY.
159
160 0283 A000       TEST3:      LDY     #0              ; ESTABLISH ADDRESSABILITY OF PIA CONTROL
161 0285 A903                   LDA     #X'03           ; REGISTER AND RESET THE CHIP
162 0287 9103                   STA     (IOBASE),Y
163 0289 A911                   LDA     #X'11           ; NEXT SET STANDARD TRANSMISSION MODE WHICH
164 028B 9103                   STA     (IOBASE),Y      ; IS 8 DATA BITS, 2 STOP BITS, NO PARITY,
165                                                     ; 16X CLOCK, AND NO INTERRUPTS.
166 028D A001                   LDY     #1              ; TRANSMIT THE FIRST CHARACTER TO FILL THE
167 028F A900                   LDA     #0              ; PIPELINE
168 0291 9103                   STA     (IOBASE),Y
169 0293 A904                   LDA     #4              ; WAIT 4 MILLISECONDS
170 0295 20E202                 JSR     TIM1MS
171 0298 A000                   LDY     #0
172 029A B103                   LDA     (IOBASE),Y      ; TEST THE TRANSMIT REGISTER EMPTY BIT IN
173 029C 2902                   AND     #X'02           ; THE STATUS REGISTER, SHOULD BE OFF
174 029E F026                   BEQ     TEST3A          ; JUMP IF NOT; NO TRANSMISSION OR TOO SLOW
175 02A0 A001                   LDY     #1              ; TRANSMIT ANOTHER CHARACTER
176 02A2 A9FF                   LDA     #X'FF
177 02A4 9103                   STA     (IOBASE),Y
178 02A6 A91D                   LDA     #29             ; WAIT 29 MILLISECONDS
179 02A8 20E202                 JSR     TIM1MS
180 02AB A000                   LDY     #0              ; TRANSMITTER BUFFER SHOULD NOT HAVE GONE
181 02AD B103                   LDA     (IOBASE),Y      ; EMPTY YET
182 02AF 2902                   AND     #X'02
183 02B1 D020                   BNE     TEST3B          ; JUMP IF IT HAS, TRANSMISSION IS TOO FAST
184 02B3 A907                   LDA     #7              ; WAIT AN ADDITIONAL 7 MILLISECONDS
185 02B5 20E202                 JSR     TIM1MS
186 02B8 B103                   LDA     (IOBASE),Y      ; TRANSMITTER BUFFER SHOULD HAVE GONE
187 02BA 2902                   AND     #X'02           ; EMPTY BY NOW
188 02BC F008                   BEQ     TEST3A          ; JUMP IF NOT, TOO SLOW
189 02BE A932                   LDA     #50             ; WAIT FOR SECOND CHARACTER TO FINISH
190 02C0 20E202                 JSR     TIM1MS
191 02C3 4CF102                 JMP     TEST4           ; GO TO NEXT TEST
192
193 02C6 A903       TEST3A:     LDA     #3              ; LOG ERROR, TEST 3
194 02C8 8500                   STA     TSTNO
195 02CA A901                   LDA     #1              ; ERROR NUMBER 1 = NO TRANSMISSION OR TOO
196 02CC 8501                   STA     ERRNO           ; SLOW
197 02CE 8502                   STA     REGAD           ; ACIA DATA REGISTER
198 02D0 4CF702                 JMP     ETEST
199
200 02D3 A903       TEST3B:     LDA     #3              ; LOG ERROR, TEST 3
201 02D5 8500                   STA     TSTNO
202 02D7 A902                   LDA     #2              ; ERROR NUMBER 2 = TRANSMISSION IS TOO FAST
203 02D9 8501                   STA     ERRNO
204 02DB A901                   LDA     #1              ; ACIA DATA REGISTER
205 02DD 8502                   STA     REGAD
206 02DF 4CF702                 JMP     ETEST
```

TEST 3 TRANSMISSION SPEED TEST

```
207
208 02E2 48        TIM1MS:  PHA                ; WAIT FOR NUMBER OF MILLISECONDS SPECIFIED
209 02E3 A98E               LDA    #1000/7     ; BY ACCUMULATOR
210 02E5 18        TIM1:    CLC                ; WAIT 1 MILLISECOND
211 02E6 69FF               ADC    #-1
212 02E8 D0FB               BNE    TIM1
213 02EA 68                 PLA                ; RETRIEVE TOTAL COUNT
214 02EB 18                 CLC                ; DECREMENT IT
215 02EC 69FF               ADC    #-1
216 02EE D0F2               BNE    TIM1MS      ; GO FOR ANOTHER MILLISECOND IF NOT
217 02F0 60                 RTS                ; RETURN IF SO
218
219
220 02F1 A900      TEST4:   LDA    #0          ; ZERO THE TEST AND ERROR NUMBERS TO
221 02F3 8500               STA    TSTNO       ; TO INDICATE NO ERRORS AND
222 02F5 8501               STA    ERRNO
223 02F7 4C221C    ETEST:   JMP    KIMMON      ; RETURN TO THE MONITOR
224
225 0000                    .END
```

NO ERROR LINES

DOCUMENTATION

```
                        .PAGE  'DOCUMENTATION'
 3                ;     BURN PROGRAM FOR M.T.U. K-1012 EPROM & I/O BOARD
 4                ;           BY KEITH SPROUL
 5
 6                ;     WILL BURN:      INTEL 2704   OR EQUIVALENT
 7                ;                       2708   OR EQUIVALENT
 8                ;                   TI TMS2716   OR EQUIVALENT
 9
10                ;     THE STARTING ADDRESS OF USER RAM HAS TO BE PUT
11                ;     INTO SAL,SAH BEFORE RUNNING ALL PARTS EXCEPT
12                ;     VERIFY NEW PROM
13
14                ;     TO BE ABLE TO PROGRAM I2704, ADDRESS LINE NINE (A9 PIN 22)
15                ;     HAS TO BE CONNECTED TO GROUND.  ALTHOUGH THE K-1012 BOARD
16                ;     WAS NOT DESIGNED TO USE THE I2704, IT CAN BE MODIFIED
17                ;     TO USE IT WITH OUT VERY MUCH DIFFICULTY.
18
19                ;     THIS PROGRAM IS WRITTEN TO PROGRAM THE I2708'S
20                ;     WITH THE DIFFERENT VALUES NEEDED FOR THE OTHER
21                ;     PROM'S SUPPLIED IN THE COMMENTS.
22
23                ;     PROM'S:       I2704  (1/2 K)
24                ;                   I2708    (1 K)
25                ;                TMS2716    (2 K)
26
27                ;     ADDRESSES OF THE I/O PORTS ARE FLAGGED WITH '********'
28                ;     IN THE COMMENTS SO THAT IT IS EASIER TO CHANGE IF THE
29                ;     BOARD IS MOVED FROM WHERE WE HAVE IT LOCATED.
30
31                ;     TO HAVE THIS PROGRAM RETURN TO THE USER'S MONITOR OR
32                ;     WHEN USED WITH SOMETHING OTHER THAN A KIM-1, CHANGE
33                ;     THE ADDRESS AT RESET FROM X'1C4F TO THE APPROPRIATE
34                ;     ADDRESS.
35
36                ;     NOTE THAT THE PROGRAM PULSE DUTY CYCLE IS 50% BECAUSE OF
37                ;     PROGRAMMING POWER LIMITATIONS AND DUTY CYCLE LIMITATIONS OF THE
38                ;     FAILSAFE CIRCUIT ON THE BOARD.  THUS IT WILL REQUIRE 200
39                ;     SECONDS TO PROGRAM A 2708.
40
```

```
0262 8501              STA    OKDATA        ; SAVE IT
0264 4C0C02            JMP    RESET         ; RETURN TO THE MONITOR

0267 20E902    OKAY:   JSR    INCTMP        ; INCREMENT REGISTERS
026A 90E0              BCC    VERFY1
026C A900              LDA    #0            ; SET ALL ERROR INFORMATION TO ZEROES IF OK
026E 8502              STA    BADADR
0270 8503              STA    BADADR+1
0272 8500              STA    BADATA
0274 8501              STA    OKDATA
0276 4C0C02            JMP    RESET         ; RETURN TO THE MONITOR

               ;       VERIFY NEW EPROM

0279 A900      NEWPRM: LDA    #X'00         ; INIT DATA PORT TO INPUT
027B 203403            JSR    INIPRT
027E 200D03            JSR    INIREG        ; RESET REGISTERS, POINTERS, & PORTB

0281 20E502    NWPRM1: JSR    LOAD          ; READ A PROM LOCATION
0284 C9FF              CMP    #X'FF         ; TEST IF IN THE ERASED STATE
0286 D014              BNE    OLDPRM        ; JUMP OUT IF NOT
0288 20E902            JSR    INCTMP        ; INCREMENT REGISTERS AND POINTERS
028B 90F4              BCC    NWPRM1        ; LOOP UNTIL ALL LOCATIONS EXAMINED

028D A900              LDA    #0            ; ZERO ALL ERROR ADDRESS IF OK
028F 8502              STA    BADADR
0291 8503              STA    BADADR+1
0293 A9FF              LDA    #X'FF         ; SET ERROR DATA TO FF IF OK
0295 8500              STA    BADATA
0297 8501              STA    OKDATA
0299 4C0C02            JMP    RESET         ; RETURN TO THE MONITOR

029C 8500      OLDPRM: STA    BADATA        ; SET BAD DATA WITH PROM CONTENTS IF NOT OK
029E A9FF              LDA    #X'FF         ; SET OKDATA TO FF
02A0 8501              STA    OKDATA
02A2 A509              LDA    TMPADR        ; SET ERROR ADDRESS IF NOT OK
02A4 8502              STA    BADADR
02A6 A50A              LDA    TMPADR+1
02A8 8503              STA    BADADR+1
02AA 4C0C02            JMP    RESET         ; RETURN TO THE MONITOR

               ;       READ EPROM CONTENTS INTO RAM

02AD A900      READ:   LDA    #X'00         ; INIT DATA PORT TO INPUT
02AF 203403            JSR    INIPRT        ; INIT PORTS
02B2 200D03            JSR    INIREG        ; INIT REGISTERS
02B5 20E502    READ1:  JSR    LOAD          ; GET PROM DATA
02B8 9109              STA    (TMPADR),Y    ; STORE IT INTO RAM
02BA 20E902            JSR    INCTMP        ; INCREMENT POINTERS
02BD 90F6              BCC    READ1         ; LOOP UNTIL DONE
02BF 4C0C02            JMP    RESET         ; RETURN TO THE MONITOR
```

```
                                .PAGE  'SUBROUTINES'
186                     ;       BURN DATA AT (TMPADR) INTO EPROM AT (ADDRESS COUNTER)
187
188 02C2 8D08FE     BURN:      STA    PORTAD        ; ********   STORE DATA AT PROM
189 02C5 AD0AFE                LDA    PORTBD        ; ********   WAIT 10 MICROSECONDS AND
190 02C8 0901                  ORA    #X'01
191 02CA EA                    NOP
192 02CB EA                    NOP
193 02CC EA                    NOP
194 02CD 8D0AFE                STA    PORTBD        ; ********   TURN ON PROGRAM PULSE
195 02D0 20DF02                JSR    DELAY         ; HOLD THE PULSE ON FOR 500 MICROSECONDS
196 02D3 AD0AFE                LDA    PORTBD        ; ********
197 02D6 29FE                  AND    #X'FE         ; TURN THE PROGRAM PULSE OFF
198 02D8 8D0AFE                STA    PORTBD        ; ********
199 02DB 20DF02                JSR    DELAY         ; HOLD IT OFF FOR 500 MICROSECONDS FOR A
200                                                  ; 50% DUTY CYCLE
201 02DE 60                    RTS                  ; RETURN
202
203 02DF A264       DELAY:     LDX    #100          ; WAIT FOR 500 MICROSECONDS
204 02E1 CA         DELAY1:    DEX
205 02E2 D0FD                  BNE    DELAY1
206 02E4 60                    RTS
207
208                     ;       LOAD DATA AT PROM (ADDRESS COUNTER) INTO ACC
209
210 02E5 AD08FE     LOAD:      LDA    PORTAD        ; ********
211 02E8 60                    RTS
212
213                     ;       INCREMENT AND TEST TMPADR, INCREMENT EPROM ADDRESS COUNTER
214
215 02E9 E609       INCTMP:    INC    TMPADR        ; INCREMENT LOW BYTE
216 02EB D002                  BNE    INC1
217 02ED E60A                  INC    TMPADR+1      ; INCREMENT HIGH BYTE IF NECESSARY
218 02EF A509       INC1:      LDA    TMPADR        ; TEST IF TMPADR IS GREATER THAN OR EQUAL
219 02F1 C506                  CMP    EAL           ; TO EAL,EAH
220 02F3 A50A                  LDA    TMPADR+1
221 02F5 E507                  SBC    EAH
222 02F7 9001                  BCC    NOTFIN        ; JUMP IF NOT
223 02F9 60                    RTS                  ; IF DONE, RETURN WITH CARRY SET
224 02FA 20FF02     NOTFIN:    JSR    INCREG        ; INCREMENT TMPADR ONLY IF NOT FINISHED
225 02FD 18                    CLC
226 02FE 60                    RTS                  ; RETURN WITH CARRY CLEAR IF NOT DONE
227
228 02FF AD0AFE     INCREG:    LDA    PORTBD        ; ****** INCREMENT HARDWARE ADDRESS COUNTER
229 0302 0904                  ORA    #X'04         ; SET INCREMENT PULSE HIGH
230 0304 8D0AFE                STA    PORTBD        ; ********
231 0307 29FB                  AND    #X'FB         ; SET INCREMENT PULSE LOW
232 0309 8D0AFE                STA    PORTBD        ; ********
233 030C 60                    RTS                  ; RETURN
234
235                     ;       INIT REGISTERS
236
237 030D 202603     INIREG:    JSR    RESADR        ; RESET ADDRESS COUNTER
238 0310 A504                  LDA    SAL           ; TRANSFER STARTING RAM ADDRESS TO TMPADR
239 0312 8509                  STA    TMPADR
```

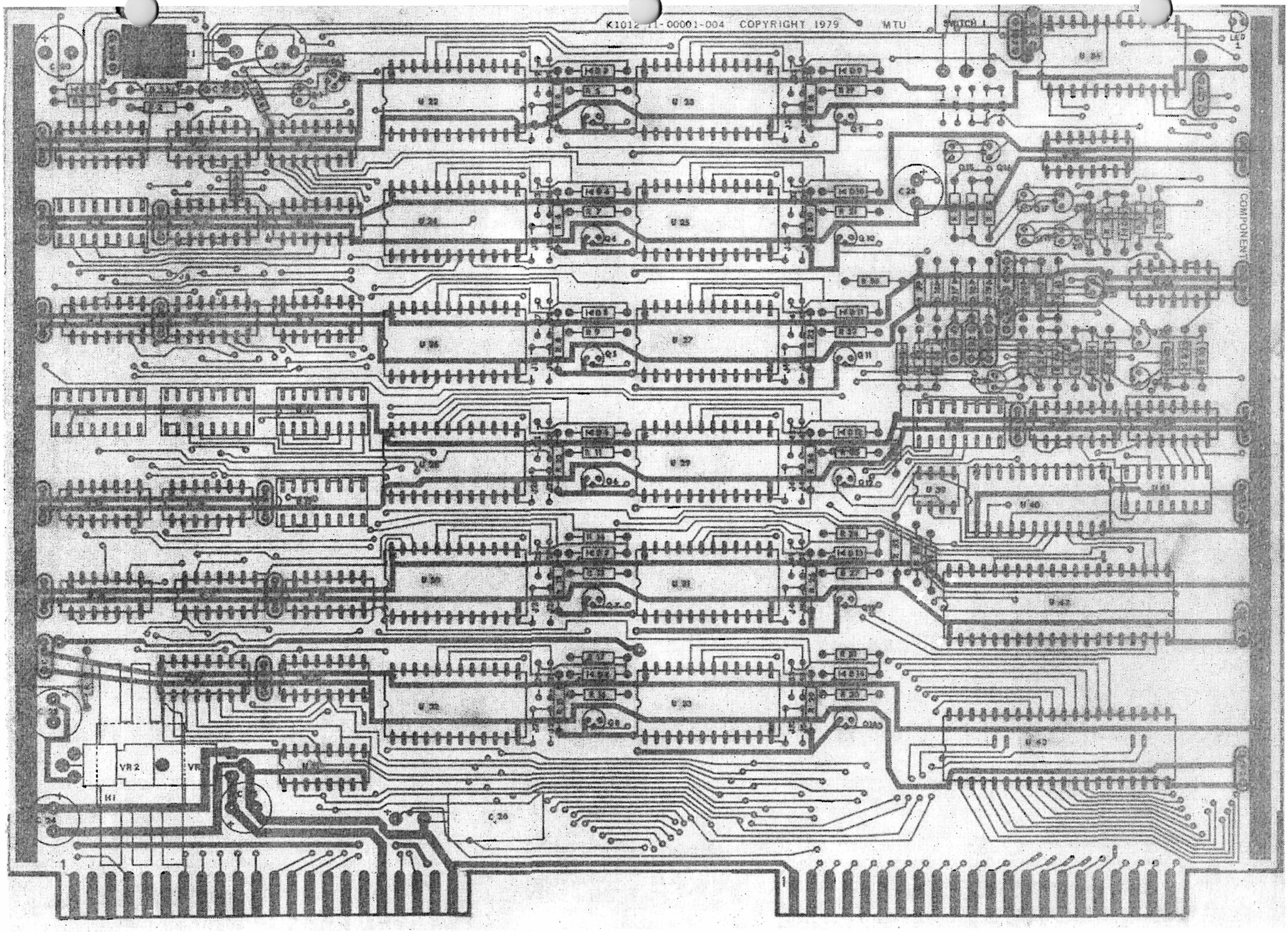
SUBROUTINES

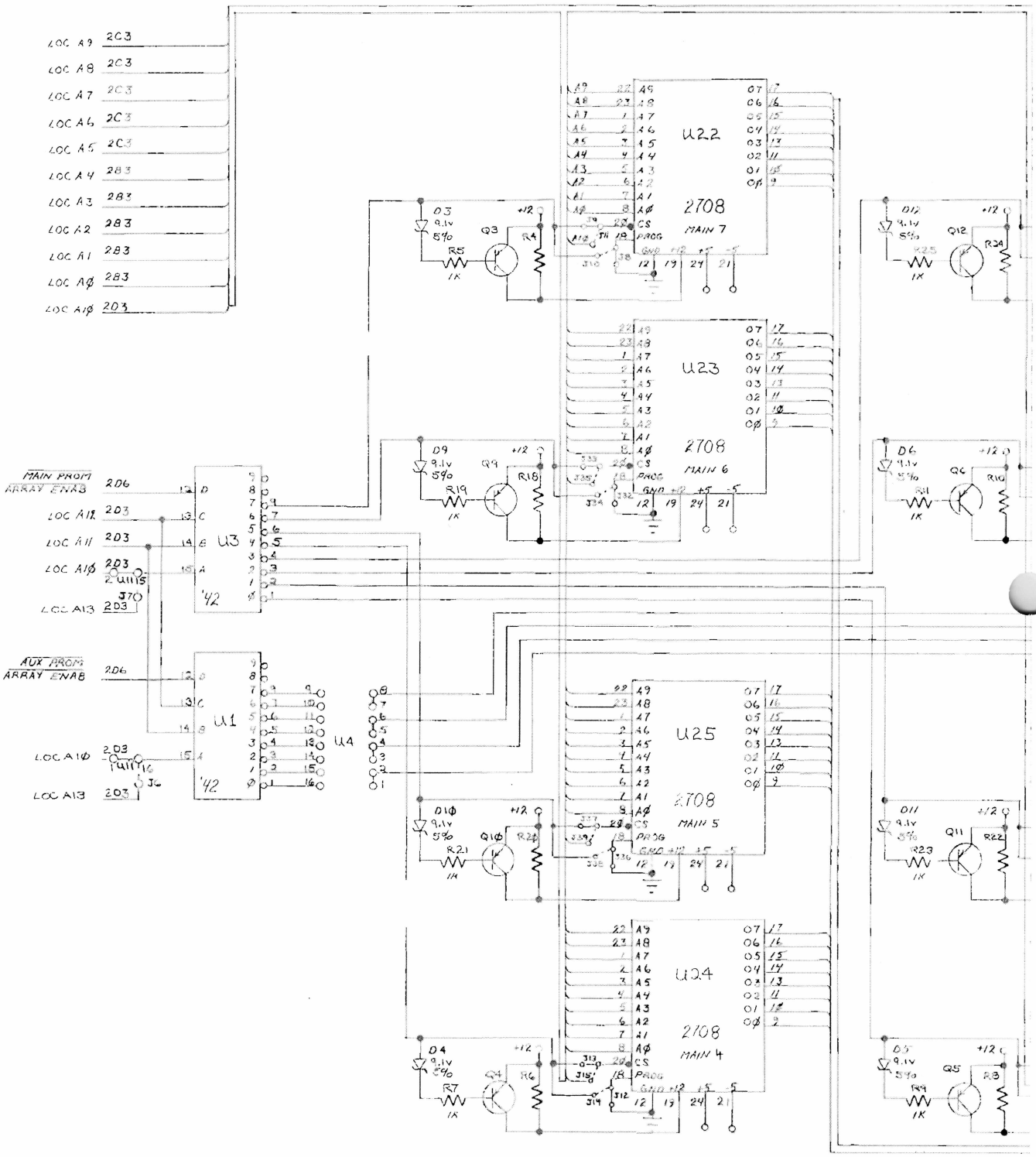
```
240 0314 A505              LDA    SAH
241 0316 850A              STA    TMPADR+1
242 0318 18                CLC                ; ADD PROM SIZE TO STARTING ADDRESS TO GET
243 0319 A504              LDA    SAL         ; ENDING ADDRESS+1
244 031B 8506              STA    EAL
245 031D A505              LDA    SAH
246 031F 6904              ADC    #4          ; 2704 = #2    TMS2716 = #8
247 0321 8507              STA    EAH
248 0323 A000              LDY    #0          ; STRAIGHT INDIRECT ADDRESSING
249 0325 60                RTS
250
251 0326 AD0AFE    RESADR: LDA    PORTBD      ; ********
252 0329 0908              ORA    #X'08       ; RESET THE HARDWARE ADDRESS COUNTER TO 0
253 032B 8D0AFE            STA    PORTBD      ; ********
254 032E 29F7              AND    #X'F7
255 0330 8D0AFE            STA    PORTBD      ; ********
256 0333 60                RTS
257
258                ;       INITIALIZE THE PORTS
259
260 0334 48        INIPRT: PHA                ; SAVE DIRECTION DATA FOR PORT A
261
262 0335 A900              LDA    #X'00       ; SET UP PORT B FOR DIRECTION REGISTER
263 0337 8D0BFE            STA    PORTBC      ; ********  ACCESS
264 033A AD0AFE            LDA    PORTBD      ; ********  SET BITS 0 - 3 TO OUTPUTS
265 033D 090F              ORA    #X'0F
266 033F 8D0AFE            STA    PORTBD      ; ********
267 0342 A904              LDA    #X'04       ; SET UP PORT B FOR DATA REGISTER ACCESS
268 0344 8D0BFE            STA    PORTBC      ; ********
269 0347 AD0AFE            LDA    PORTBD      ; ********  SET IDLE STATE OF PROM CONTROL
270 034A 29F0              AND    #X'F0       ; BITS
271 034C 0902              ORA    #X'02       ; NO RESET, NO INCREMENT, READ MODE, NO
272                                           ; PROGRAM PULSE
273                                           ; X'00 FOR TMS2716
274 034E 8D0AFE            STA    PORTBD      ; ********
275
276 0351 A900              LDA    #X'00       ; SET UP PORT A FOR DIRECTION REGISTER
277 0353 8D09FE            STA    PORTAC      ; ******** ACCESS
278 0356 68                PLA                ; RESTORE DESIRED A DIRECTION DATA
279 0357 8D08FE            STA    PORTAD      ; ******** SET UP DIRECTION DATA
280 035A A904              LDA    #X'04       ; SET UP PORT A FOR DATA REGISTER ACCESS
281 035C 8D09FE            STA    PORTAC      ; ********
282
283 035F 60                RTS                ; RETURN
284
285 0000                   .END
```

NO ERROR LINES

K-1012 PARTS LIST

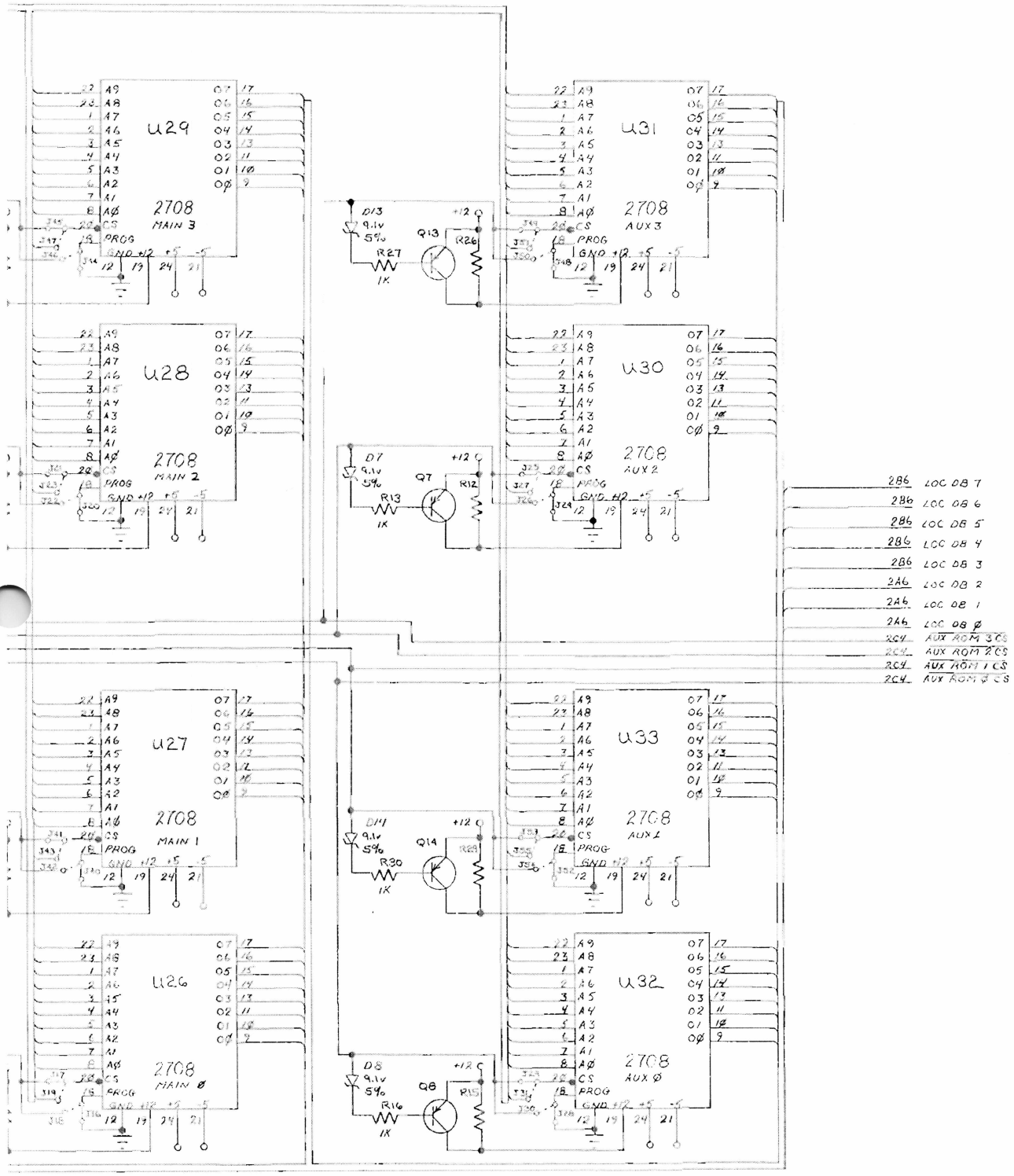
PART DESCRIPTION	QUANTITY	DESIGNATORS
LOGIC 74LS00	1	U5
LOGIC 74LS04	3	U13,17,18
LOGIC 74LS08	2	U14,16
LOGIC 74LS10	1	U9
LOGIC 74LS26	2	U2,44
LOGIC 74LS30	3	U6,7,8
LOGIC 74LS42	2	U1,3
LOGIC 74LS161	1	U37
LOGIC 74LS367	3	U19,20,21
LOGIC 74LS393	1	U38
LOGIC 1458	1	U39
LOGIC 6520	2	U42,43
LOGIC 6850	1	U40
LOGIC CD4040	1	U35
VOLT REG 340T5	1	VR3
VOLT REG 320T5	1	VR1
VOLT REG 342P12	1	VR2
CAP ELECT 16V 100UF	5	C20,21,23,24,25
CAP ELECT 25V 1000UF	1	C26
CAP ELECT 35V 47UF	1	C28
CAP POLY 25V 1000PF 5%	1	C27
CAP Z5U 12V .05UF	22	C1-19, C22, C34, C35
CAP Z5U 12V .1UF	4	C29,30,31,32
CAP Z5U 25V .1UF	1	C33
HEAT SINK 1W TO-220	1	H1
DIODE SIL SIGNAL 1N914	10	D1,2,16-23
DIODE GER SIGNAL 1N270	2	D24,25
DIODE ZENER .4MW 9.1V	12	D3-14
DIODE ZENER 1W 24.5V 2%	1	D15
DIODE LED RED	1	LED-1
TRANS PNP SIG 2N2907	16	Q1,3-15,17,18
TRANS NPN SIG 2N2222	5	Q2,16,19,20,21
TRANS NPN SIG 2N3646	3	Q22,23,24
RES 1/4W 5% 27	2	R34,36
RES 1/4W 5% 270	2	R53,54
RES 1/4W 5% 470	1	R33
RES 1/4W 5% 1K	13	R5,7,9,11,13,16,19,21,23,25,27,30,55
RES 1/4W 5% 1.5K	1	R1
RES 1/4W 5% 4.7K	2	R37,40
RES 1/4W 5% 10K	19	R2,R3,14,17,28,31,32,39,41-52,56
RES 1/4W 5% 27K	1	R35
SOCKET PC 16P	7	XU4,10,11,12,15,36,41
SOCKET PC 24P	14	XU22-34,40
SOCKET PC 40P	2	XU42,43
SWITCH SPST PC TOGGLE OR SLIDE	1	SW1
PC BOARD K-1012	1	PCB1
SCREW 4-40 3/8	1	
SCREW 4-40 1/2	1	
NUT 4-40	2	
WASHER, FIBRE 4-40	1	
TRICKLE RESISTORS ON PROMS IF NEEDED		R4,6,8,10,12,15,18,20,22,24,26,29


K1012-11-0001-004 COPYRIGHT 1979 MTU
SWITCH
COMPONENT
VR2
VR1
H1
C36

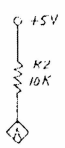


NOTES: 1. DIODES ON THIS PAGE ARE 9.1V 5% 400MW
2. TRANSISTORS THIS PAGE ARE PN2907
3. ALL TTL IC'S ARE LOW POWER SHOTTKY UNLESS OTHERWISE NOTED
4. SOLID LINES BETWEEN JUMPERS ARE FOR 2708
DOTTED LINES BETWEEN JUMPERS ARE FOR 2716

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



RWISE SPECIFIED



TOLERANCES UNLESS OTHERWISE SPECIFIED		PROM-I/O BOARD	
FRACTIONS DEC ANGLES			
± ± ±			
APPROVALS	DATE	MICRO TECHNOLOGY UNLIMITED	
DRAWN DBC	10/20/78		
CHECKED		SCALE	SIZE D
		DRAWING NO. K-1012	
		DO NOT SCALE DRAWING	SHEET 1 of 3